Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1-19. (Canceled)

20. (Previously Presented) An integrated circuit using a memory, said integrated circuit comprising:

an interface circuit configured to control access to said memory, said interface circuit coupled to said memory;

an embedded processor configured to control said integrated circuit, said embedded processor receiving information from said interface circuit; and

an array processor for performing mathematical calculations on data received from said interface circuit and connected to said embedded processor via an internal bus, said array processor comprising:

a plurality of multiplier/accumulator circuits;

a plurality of shared operand circuits coupled to said plurality of multiplier/accumulator circuits for simultaneously providing a shared operand to at least two of said plurality of multiplier/accumulator circuits; and

a shared output and feedback interface coupled to receive outputs from the at least two of the plurality of multiplier/accumulator circuits and to provide them for further processing by the at least two of the multiplier/accumulator circuits,

wherein each of the plurality of shared operand circuits comprise:

a front end unit for determining a fixed point result by performing a fixed point addition or subtraction on a plurality of operands; and

a floating point conversion unit for converting said fixed point result to a first floating point result.

21-22. (Canceled)

23. (Currently Amended) An integrated circuit comprising:

a first embedded processor;

a first array processor coupled to the first embedded processor;

a first memory interface circuit coupled to the first embedded processor and the first array processor;

a first communication port coupled to the first embedded processor;

a second communication port configured to communicate with the first communication port;

a second embedded processor coupled to the second communication port;

a second array processor coupled to the second embedded processor; and

a second memory interface circuit coupled to the second embedded processor and the second array processor,

wherein the first array processor comprises at least two arithmetic processing units, each of the at least two arithmetic processing units comprises:[[.]]

a first MAC unit coupled to a first local memory;

a second MAC unit coupled to a second local memory;

a third MAC unit coupled to a third local memory;

~~a fourth MAC unit coupled to a fourth local memory;~~

a shared operand unit coupled to provide a shared operand to the first MAC unit, the second MAC unit, and the third MAC unit~~, and the fourth MAC unit~~; and

a shared output and feedback interface coupled to receive a first output from the first MAC unit, a second output from the second MAC unit, and a third output from the third MAC unit, ~~and a fourth output from the fourth MAC unit~~ and further coupled to provide the first output to the first local memory, the second output to the second local memory, and the third output to the third local memory~~, and the fourth output to the fourth local memory~~.

24. (Canceled)

25. (Currently Amended) ~~An~~ The integrated circuit of claim 23 wherein the at least two arithmetic processing units are three arithmetic processing units. ~~comprising:~~

~~a first embedded processor;~~

~~a first array processor coupled to the first embedded processor;~~

~~a memory interface circuit coupled to the first embedded processor and the first array processor;~~

~~a first communication port coupled to the first embedded processor and the first array processor for communicating with a second array processor and a second embedded processor;~~

~~wherein the first array processor comprises:~~

~~a first MAC unit coupled to a first local memory;~~

~~a second MAC unit coupled to a second local memory;~~

~~a shared output and feedback interface coupled to receive a first output from the first MAC unit and a second output from the second MAC unit and further coupled to provide the first output and the second output to the first and second local memories; and~~

~~a shared operand unit coupled to the first MAC unit and the second MAC unit, the shared operand unit for simultaneously providing a shared operand to the first MAC unit and the second MAC unit.~~

26. (Currently Amended) The integrated circuit of claim [[25]]23 wherein each of the at least two arithmetic processing units further comprises a fourth MAC unit coupled to a fourth local memory. ~~the first communication port communicates with a second communication port, the second communication port coupled to the second embedded processor.~~

27. (Currently Amended) An integrated circuit comprising:

an interface circuit configured to receive data from an external memory;

a first embedded processor configured to control the interface circuit;

a first array processor configured to receive data from the interface and to perform arithmetic calculations;

a first communication port coupled to the first embedded processor and the first array processor for communicating with a second array processor and a second embedded processor,

the array processor comprising:

a first MAC unit configured to receive data from a first local memory;

a second MAC unit configured to receive data from a second local memory; ~~and~~

a third MAC unit configured to receive data from a third local memory;

a first shared output and feedback circuit configured to receive data from the first MAC unit, ~~and~~ the second MAC unit, and third MAC unit, and further configured to provide data to the first local memory, ~~and~~ the second local memory, and the third local memory;

a fourth MAC unit configured to receive data from a fourth local memory;

a fifth MAC unit configured to receive data from a fifth local memory; and

a second shared output and feedback circuit configured to receive data from the fourth MAC unit and the fifth MAC unit, and further configured to provide data to the fourth local memory and the fifth local memory.

28. (Currently Amended) The integrated circuit of claim 27 wherein the array processor further comprises:

a first shared operand circuit configured to simultaneously provide a shared operand to the first MAC unit, ~~and~~ the second MAC unit, and the third MAC unit.

29. (Canceled)

30. (Currently Amended) The integrated circuit of claim 28 wherein the array processor further comprises:

~~a third MAC unit configured to receive data from a third local memory;~~

~~a fourth MAC unit configured to receive data from a fourth local memory;~~

~~a second shared output and feedback circuit configured to receive data from the third MAC unit and the fourth MAC unit, and further configured to provide data to the fourth first local memory, the second local memory, the third local memory, and the fourth local memory; and~~

a second shared operand circuit configured to simultaneously provide a shared operand to the fourth ~~third~~ MAC unit and the fifth ~~fourth~~ MAC unit.

31. (Currently Amended) A frame rendering integrated circuit comprising:

an interface circuit coupled to an external memory;

an embedded processor coupled to the interface circuit and configured to control the integrated circuit; and

an array processor coupled to the interface circuit, wherein the array processor performs arithmetic calculations;

wherein the array processor comprises:

a first multiply/accumulator (MAC) unit coupled to a first local memory, the first local memory comprising a first plurality of operands;

a second MAC unit coupled to a second local memory, the second local memory comprising a second plurality of operands;

a third ~~multiply/accumulator (MAC)~~ MAC unit coupled to a third local memory, the third local memory comprising a third plurality of operands;

a fourth MAC unit coupled to a fourth local memory, the fourth local memory comprising a fourth plurality of operands; ~~and~~

a fifth MAC unit coupled to a fifth local memory, the fifth local memory comprising a fifth plurality of operands;

a sixth MAC unit coupled to a sixth local memory, the sixth local memory comprising a sixth plurality of operands;

a first shared operand unit coupled to the first MAC unit, the second MAC unit, and the third MAC unit, ~~and the fourth MAC unit,~~ and

a second shared operand unit coupled to the fourth MAC unit, the fifth MAC unit, and the sixth MAC unit.

32. (Currently Amended) The integrated circuit of claim 31 wherein the array processor further comprises:

a first shared output and feedback interface coupled to the first MAC unit, the second MAC unit, and the third MAC unit, ~~and the fourth MAC unit,~~ and further coupled to the first local memory, the second local memory, and the third local memory~~, and the fourth local memory~~.

33. (Currently Amended) The integrated circuit of claim 32 wherein the shared operand provides a shared operand to the first MAC unit for computing a first result in association with the first plurality of operands, to the second MAC unit for computing a second result in association with the second plurality of operands, and to the third MAC unit for computing a third result in association with the third plurality of operands~~, and to the fourth MAC unit for computing a fourth result in association with the fourth plurality of operands~~.

34. (Currently Amended) The integrated circuit of claim 33 wherein the first result, the second result, and the third result~~, and the fourth result~~ are computed independently of each other.

35. (Currently Amended) The integrated circuit of claim 34 wherein the first shared output and feedback interface receives the first result from the first MAC unit, the second result from the second MAC unit, and the third result from the third MAC unit, ~~and the fourth result from the fourth MAC unit,~~ and provides the first result to the first local memory, the second result to the second local memory, and the third result to the third local memory~~, and the fourth result to the fourth local memory~~.

36. (New) The integrated circuit of claim 31 wherein the array processor further comprises:

a second shared output and feedback interface coupled to the fourth MAC unit, the fifth MAC unit, and the sixth MAC unit, and further coupled to the fourth local memory, the fifth local memory, and the sixth local memory.